Claims

1. (Currently Amended) A manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region and an active region, electrically isolated by the element isolation region, on a semiconductor layer; [[and]]

(b) forming a [[resistive impurity]] resistor layer[[, at least,]] in [[a part of]] the active region ~~by forming a first impurity-doping region, and providing a first impurity-doping forbidden region in the element isolation region at the same time;~~

(c) forming a gate insulation layer on the semiconductor layer;

(d) forming a gate electrode layer on the gate insulation layer; and

(e) forming at least one contact layer connected to the resistor layer, a source and a drain in the semiconductor layer simultaneously.

2. (Currently Amended) [[The]] A manufacturing method of [[the]] a semiconductor device ~~according to claim 1, wherein a plurality of the resistive impurity layers are formed, and the first impurity-doping forbidden region is formed so as to isolate the adjacent first impurity-doping regions in the (b)~~ comprising:

(a) forming an element isolation, a first active region and a second active region on a semiconductor layer, the first active region and the second active region being electrically isolated by the element isolation region respectively;

(b) forming a first resistor layer in the first active region and a second resistor layer in the second active region;

(c) forming a gate insulatation layer on the semiconductor layer;

(d) forming a gate electrode layer on the gate insulation layer;

(e) forming a first contact layer connected to the first resistor layer, a second contact layer connected to the second resistor layer, a source and a drain in the semidconductor layer simultaneously.

3. (Currently Amended) The manufacturing method of the semiconductor device

according to [[claim 1 or]] claim 2, further comprising;

before step (e), forming a resist layer which has a first opening at least above a termination of the first resistor layer and a second opening at least above a termination of a second resistor layer, the first opening and the second opening of the resist layer being continuous ~~forming a contact impurity layer by forming a second impurity-doping region in a region, continuously connected to the resistive impurity layer~~.

4. (Currently Amended) The manufacturing method of the semiconductor device according to claim [[3]] 1 or 2, wherein the element isolation region is semi-recessed LOCOS ~~a second impurity-doping forbidden region is provided, at least, in the element isolation region when forming the second impurity-doping region~~.

Please cancel claims 5-22 without prejudice or disclaimer.

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)